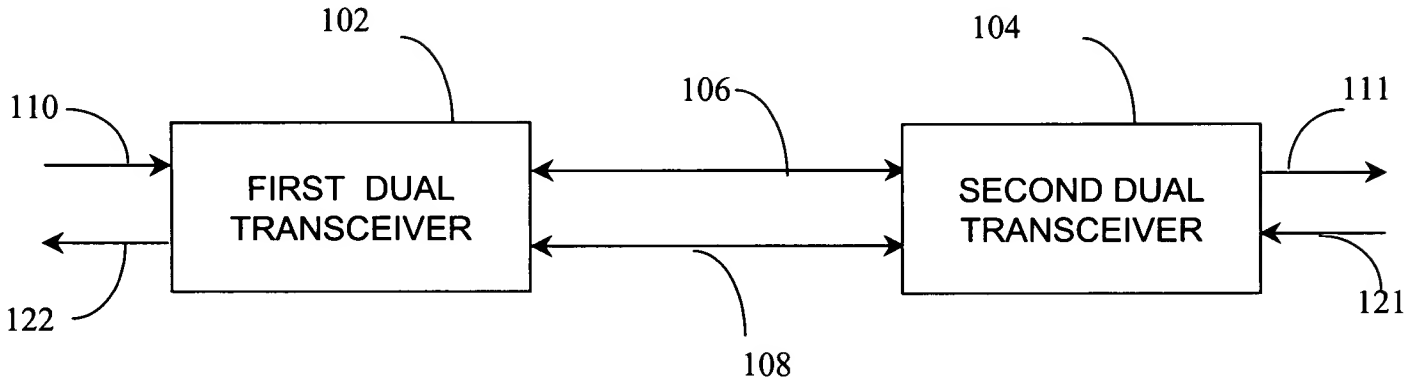

102
104
110
106
111
FIRST DUAL TRANSCEIVER
SECOND DUAL TRANSCEIVER
122
121
108

Fig. 1

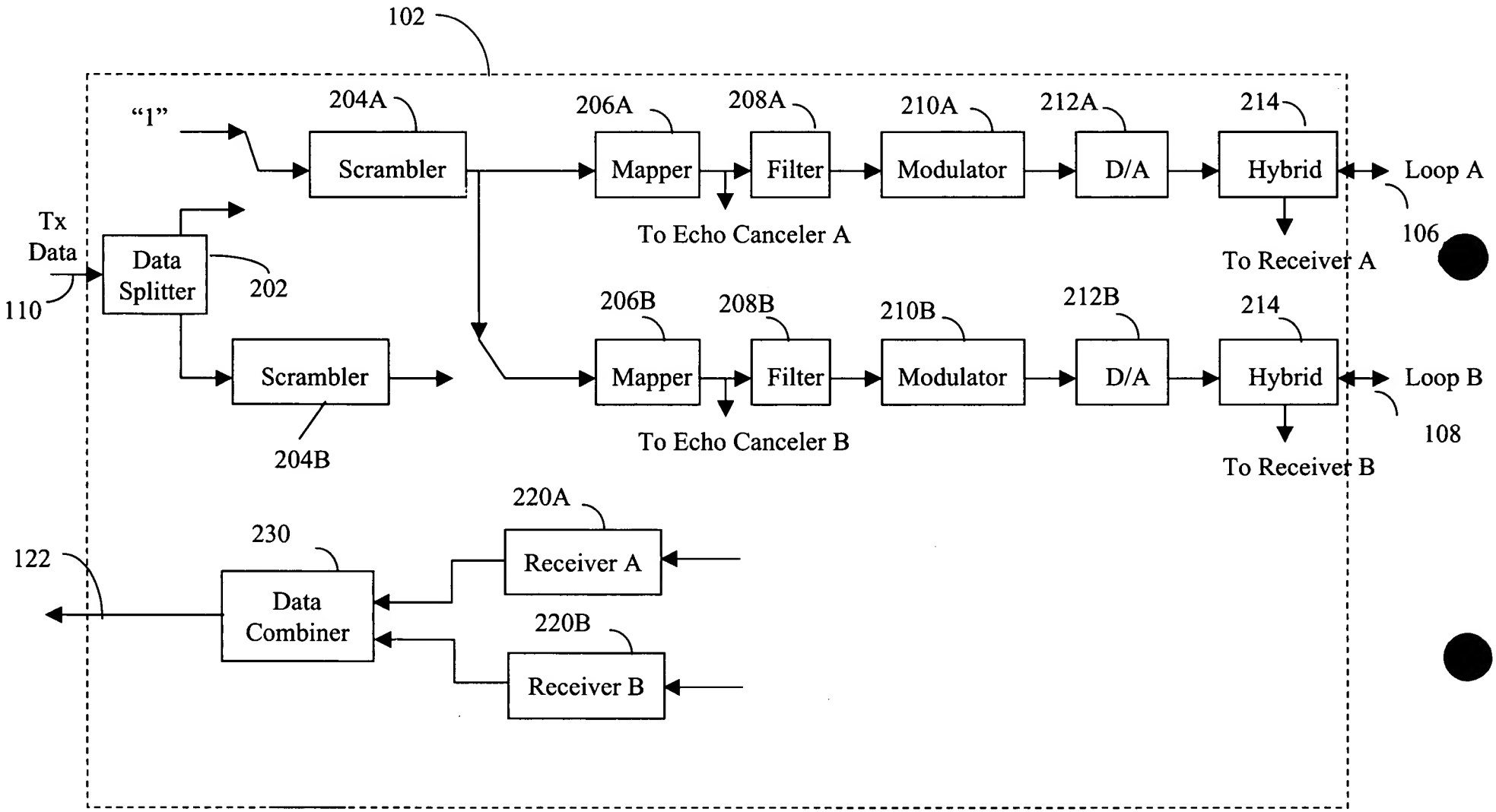

102
"1"
204A
Scrambler
206A
Mapper
208A
Filter
210A
Modulator
212A
D/A
214
Hybrid
Loop A
106
To Echo Canceler A
To Receiver A
Tx Data
110
Data Splitter
202
Scrambler
204B
206B
Mapper
208B
Filter
210B
Modulator
212B
D/A
214
Hybrid
Loop B
108
To Echo Canceler B
To Receiver B
220A
Receiver A
230
122
Data Combiner
220B
Receiver B

FIG. 2

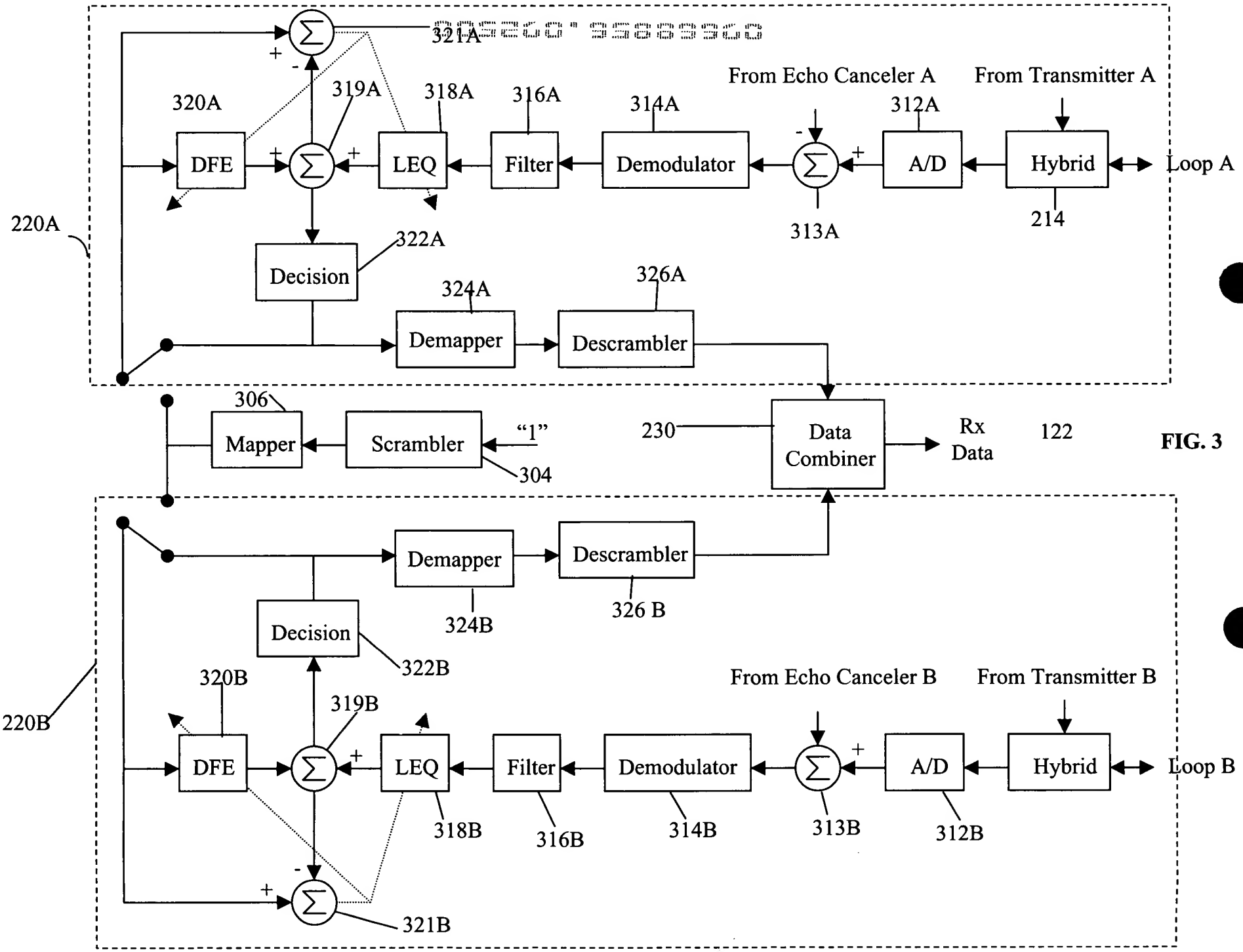

321A
From Echo Canceler A
From Transmitter A
320A
319A
318A
316A
314A
312A
DFE
LEQ
Filter
Demodulator
A/D
Hybrid
Loop A
313A
214
220A
322A
Decision
324A
326A
Demapper
Descrambler
306
Mapper
Scrambler
"1"
304
230
Data Combiner
Rx Data
122
Demapper
Descrambler
324B
326 B
Decision
322B
320B
319B
From Echo Canceler B
From Transmitter B
220B
DFE
LEQ
Filter
Demodulator
A/D
Hybrid
Loop B
318B
316B
314B
313B
312B
321B

FIG. 3

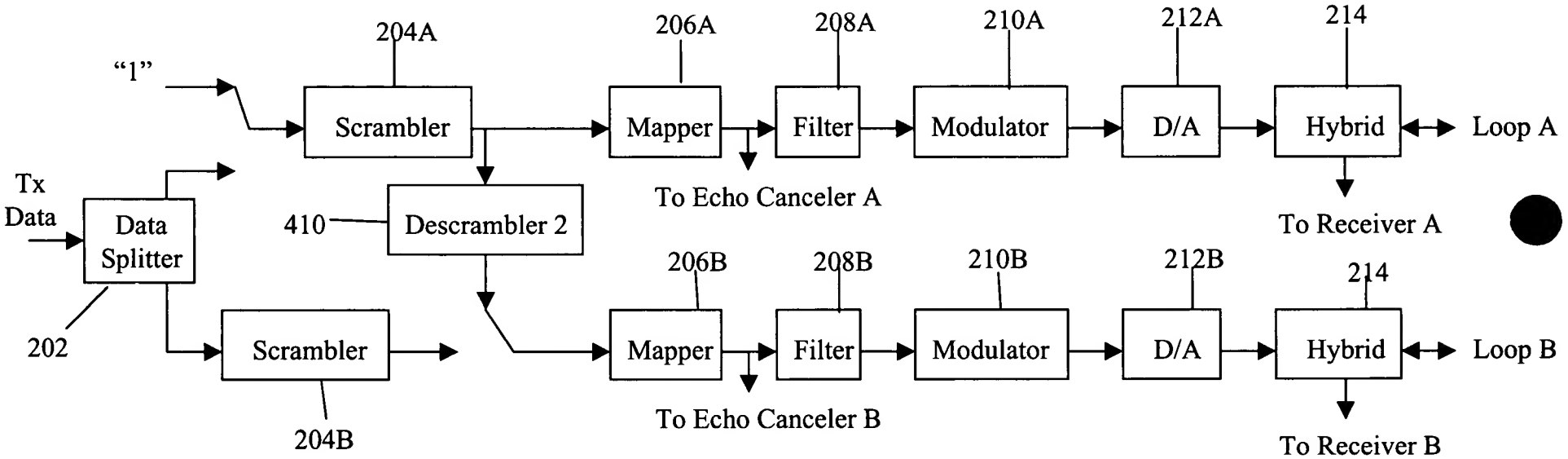

"1"
204A
206A
208A
210A
212A
214
Scrambler
Mapper
Filter
Modulator
D/A
Hybrid
Loop A
To Echo Canceler A
To Receiver A
Tx
Data
Data
Splitter
410
Descrambler 2
206B
208B
210B
212B
214
202
Scrambler
Mapper
Filter
Modulator
D/A
Hybrid
Loop B
To Echo Canceler B
To Receiver B
204B

FIG. 4

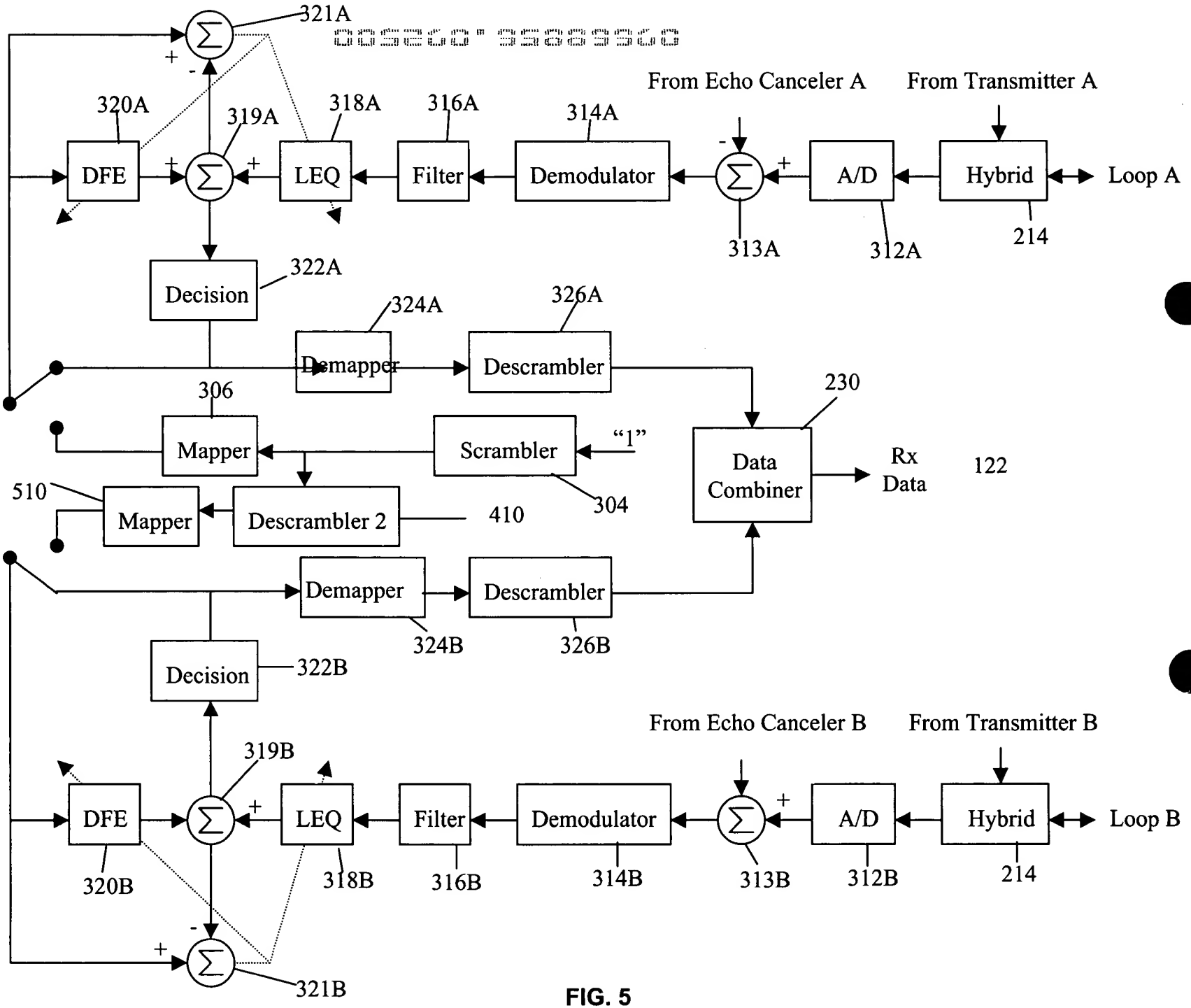
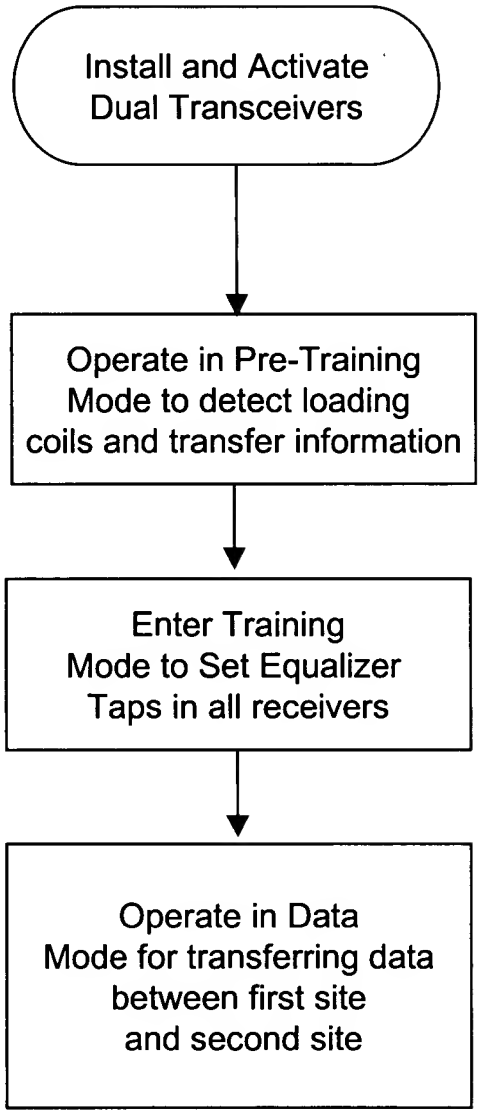

321A
From Echo Canceler A
From Transmitter A
320A
319A
318A
316A
314A
DFE
LEQ
Filter
Demodulator
A/D
Hybrid
Loop A
313A
312A
214
Decision
322A
324A
326A
Demapper
Descrambler
306
230
Mapper
Scrambler
"1"
Data Combiner
Rx Data
122
510
Mapper
Descrambler 2
410
304
Demapper
Descrambler
324B
326B
Decision
322B
From Echo Canceler B
From Transmitter B
319B
DFE
LEQ
Filter
Demodulator
A/D
Hybrid
Loop B
320B
318B
316B
314B
313B
312B
214
321B

FIG. 5

FIG. 6


Install and Activate Dual Transceivers
Operate in Pre-Training Mode to detect loading coils and transfer information
Enter Training Mode to Set Equalizer Taps in all receivers
Operate in Data Mode for transferring data between first site and second site

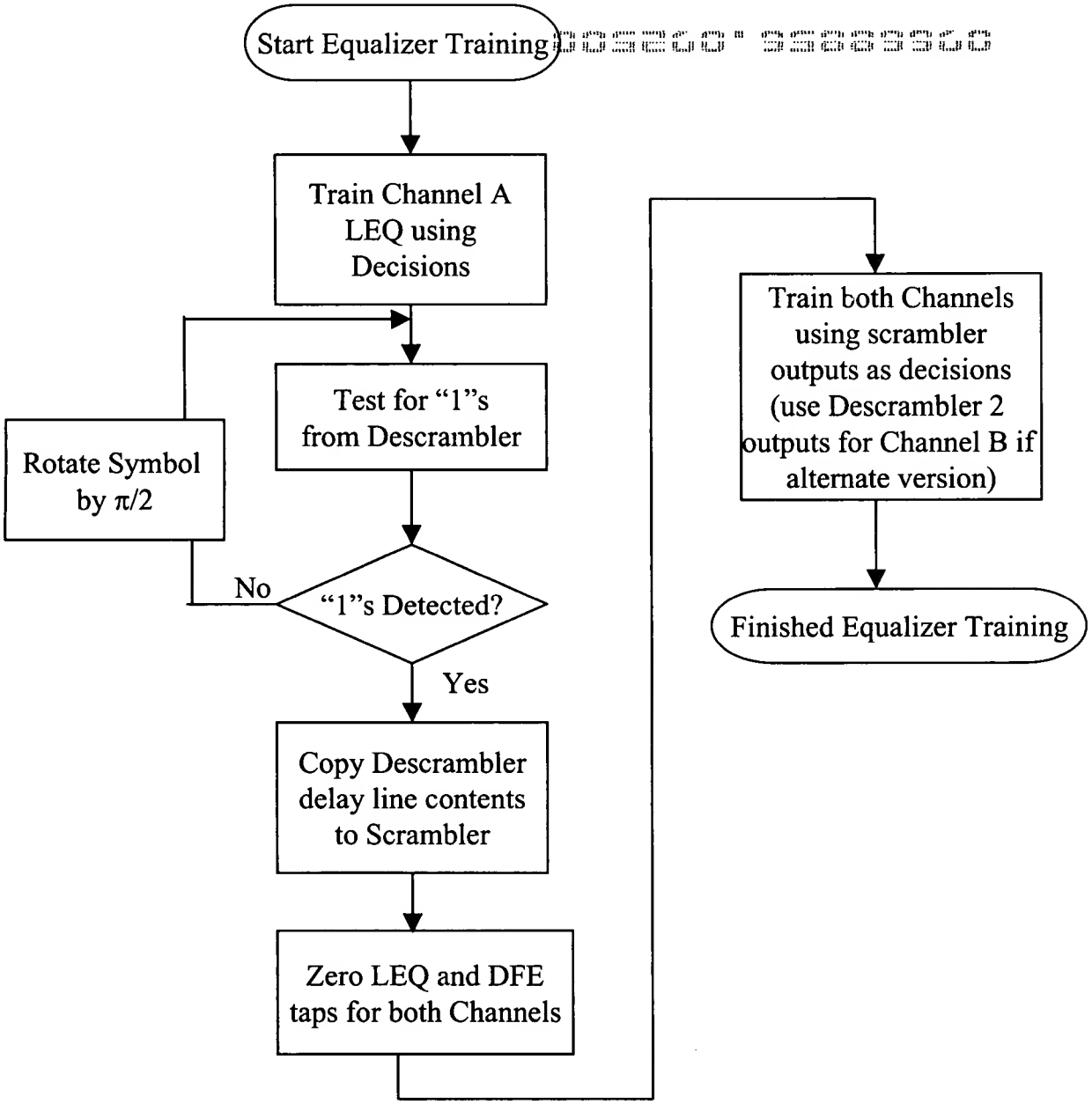

Start Equalizer Training
Train Channel A LEQ using Decisions
Test for "1"s from Descrambler
Rotate Symbol by π/2
No
"1"s Detected?
Yes
Copy Descrambler delay line contents to Scrambler
Zero LEQ and DFE taps for both Channels
Train both Channels using scrambler outputs as decisions (use Descrambler 2 outputs for Channel B if alternate version)
Finished Equalizer Training

FIG. 7

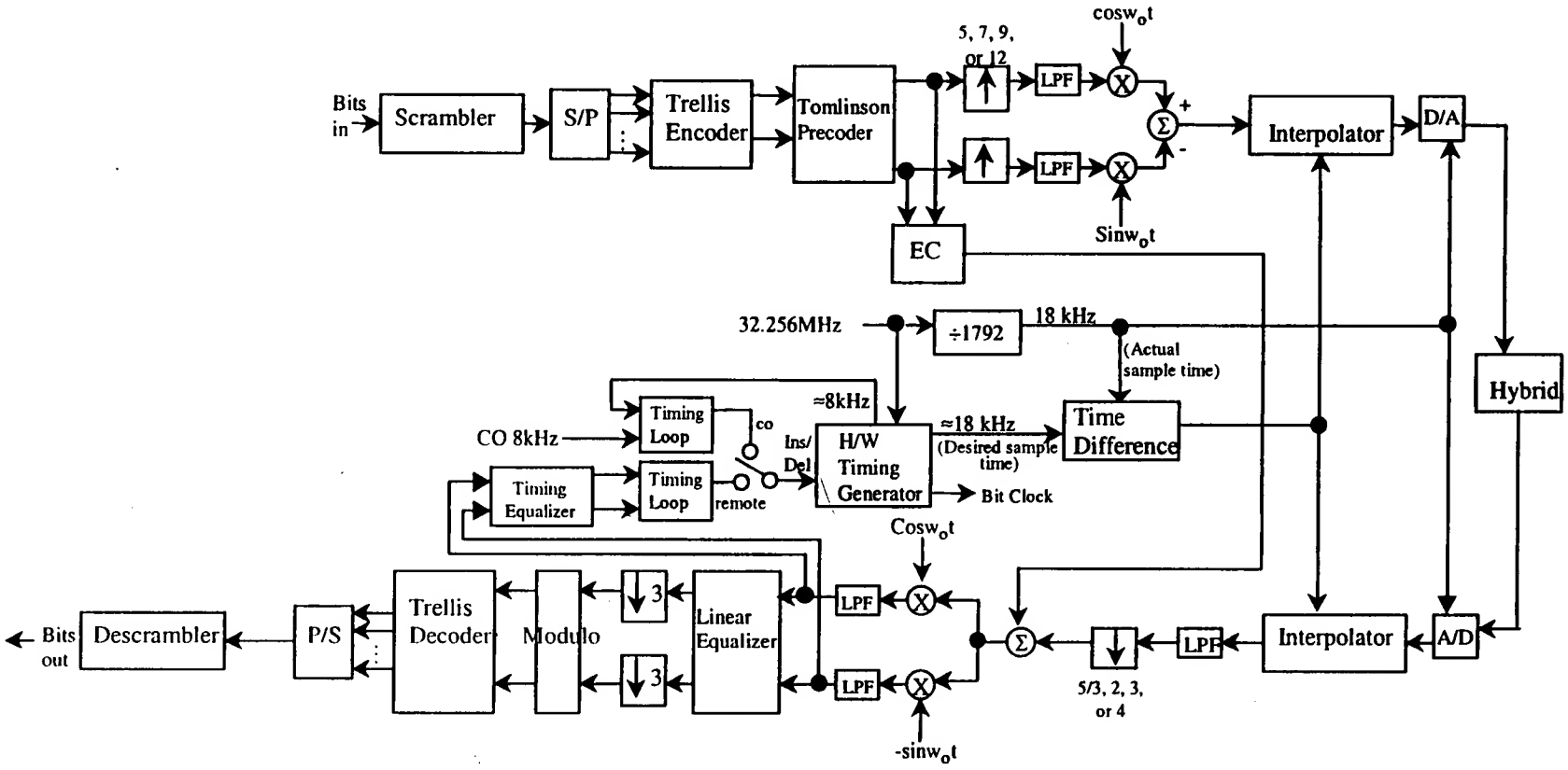

Bits in
Scrambler
S/P
Trellis Encoder
Tomlinson Precoder
5, 7, 9, or 12
LPF
LPF
cosw$_o$t
Sinw$_o$t
+
-
Interpolator
D/A
Hybrid
EC
32.256MHz
÷1792
18 kHz
(Actual sample time)
≈8kHz
Timing Loop
CO 8kHz
co
Ins/ Del
H/W Timing Generator
≈18 kHz
(Desired sample time)
Time Difference
Timing Equalizer
Timing Loop
remote
Bit Clock
Cosw$_o$t
Bits out
Descrambler
P/S
Trellis Decoder
Modulo
3
3
Linear Equalizer
LPF
LPF
5/3, 2, 3, or 4
Interpolator
A/D
-sinw$_o$t

FIG. 8